UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/030,252	01/09/2002	Tetsuro Yoshimoto	60188-141	1962

20277 7590 01/30/2003

MCDERMOTT WILL & EMERY
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
KOYAMA, KUMIKO C	
ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 01/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,252	YOSHIMOTO ET AL.	
	Examiner	Art Unit	
	Kumiko C. Koyama	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) 3 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Preliminary Amdt/Amendment

1. Acknowledgment is made of Preliminary Amendment filed on January 9, 2002.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the analog circuit part must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because it includes reference numbers. The examiner respectfully requests the applicant to eliminate the references numbers in the abstract.

Claim Objections

4. Claims 1-8 are objected to because of the following informalities:

The examiner respectfully requests the applicant to fully spell out all the abbreviations in the claims. For example,

Re claim 1, line 1: "IC" should be changed to --Integrated Circuit--.

Re claim 1, line 7: "DMA" should be changed to --Direct Memory Access--.

Re claim 1, line 12: "CPU" should be changed to --central processing unit--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al (US 4,962,485) in view of Copeland, III et al (US 5,179,661) and Tanaka (US 4,924,075).

Kato discloses a contactless IC card that sends/receives data to/from the ourside and is supplised with power from the outside in a contactless manner and comprises a transmission circuit for sending/receiving data to/from the outside (col 1 lines 66+), a RAM, a nonvolatile memory (col 1 line 17), a CPU for executing write/read processing on the memory (col 1 lines 16-19, lines 29-33).

Kato fails to disclose a DMA circuit for transmitting data received by the transmission circuit to the buffer memory and transmitting data stored in the buffer memory to the transmission circuit and state control means for halting operations of the nonvolatile memory and the CPU while the transmission circuit is sending/receiving data to/from the outside.

Copeland teaches buffers and a DMA data transfer of data between a memory and the buffer (col 4 lines 44-50).

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to integrate the teachings of Copeland to the teachings of Kato because DMA provides a high speed data exchange between the IC card reader/writer and the IC card, therefore provides faster service.

Tanaka teaches a state control means for halting operations of the CPU 27 (col 4 lines 15-16). Tanaka also teaches that the CPU 27 selectively executes the programs in program memory 28 (col 4 lines 29-35).

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to integrate the teachings of Tanaka to the teachings of Kato as modified by Copeland and have a state control means for halting operations of the nonvolatile memory and the CPU while transmission circuit is sending/receiving data to/from the outside so that unnecessary battery is not used and avoid possible data error, which provides a more accurate data transfer.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato as modified by Copeland and Tanaka as applied to claim 1 above, and further in view of Yorimoto et al (US 5,129,091).

Copeland teaches that 9600 bits per second are transmitted (col 1 lines 34-39).

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to modify the teachings of Copeland to the teaching of Kato as modified by Copeland and Tanaka as discussed above in claim 1 and provide a data bit appearing every

predetermined period in data sent/received by the transmission circuit in order to accurately transmit data to/from the IC card with high speed.

Kato/Copeland/Tanaka fail to teach that the transmission circuit generates an interruption signal at timing between a period for sending/receiving one data bit and a period for sending/receiving another data bit, and the DMA circuit executes transmission processing in response to the interruption signal.

Yorimoto teaches a request for interrupt to the microprocessor unti 22 is not accepted when data is being loaded into the memory 24 during data write cycle of the microprocessor unit 22.

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to integrate the modify the teachings of Yorimoto the teachings of Kato/Copeland/Tanaka so that the transmission circuit generates an interruption signal between a period for sending/receiving one data bit and a period for sending/receiving another data bit in order to accurately acquire the transmitting data with out any distortion caused by the interruption, therefore avoiding any erroneous data.

8. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato as modified by Copeland and Tanaka as applied to claim 1 above, and further in view of Ohno (US 6,045,042) and Kim et al (US 5,729,004). Kato/Copeland/Tanaka have been discussed above.

Kato/Copeland/Tanaka fail to teach that data received by the transmission circuit has a structure in accordance with the standard of ISO/IEC 14443-3, the transmission circuit includes an analog circuit part for modulating a data received from the outside into a digital data and outputting the digital data, the IC card further comprises preset signal generation means for

giving the analog circuit part a preset signal that is active during a period other than a period when the transmission circuit is receiving a data, and the analog circuit part sets an output thereof to an logical high level in response to the active preset signal.

The admitted prior art discloses the ISO 14443-3 in the Background Art section of the application and the standard ISO 14443-3 was known by others before the applicant's invention. Furthermore, the it discloses that "contactless IC cards under development in various companies are to comply with the anti-collision function of ISO 14443-3 for allowing one reader/writer to simultaneously write/read data in/from a plurality of IC cards."

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to modify the teachings of Kato/Copeland/Tanaka and have an IC card that is compliant to 14443-3 in order to transfer data to multiple IC cards without having erroneous data transfer.

Ohno teaches that an external signal is detected and converted from an analog signal to a digital signal by the demodulator.

Therefore, it would have been obvious to an artisan of ordinary sill in the art at the time the invention was made to integrate the teachings of Ohno to the teachings of Kato/Copeland/Tanaka because digital data are more distinct, which causes less error during signal processing and analyzing, and are more easily carried out since the data is either 1 or 0, which makes the process faster.

Kim teaches that the start bit is a logic "low" level, and the terminal SIO goes from the logic "high" level to the logic "low" level when the card reader starts a data transmission.

Therefore, it would have been obvious to an artisan of ordinary sill in the art at the time the invention was made to integrate the teachings of Kim to the teachings of Kato/Copeland/Tanaka/Ohno so that the data transmission is not prevented or interrupted by other operation by the card and provides the opportunity to process the signal after the transmission is complete, which prevents erroneous data transfer and processing of the received signals.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato as modified by Copeland and Tanaka as applied to claim 1 above, and further in view of Arai (US 5,845,134). Kato/Copeland/Tanaka have been discussed above.

Kato/Copeland/Tanaka fail to teach an IC card comprising a resume circuit for storing, when data write processing on the nonvolatile memory executed by the CPU is interrupted, a proceeding state of the write processing up to time of interruption, wherein the CPU resumes the write processing on the nonvolatile memory on the basis of the proceeding state stored in the resume circuit.

Arai teaches a resume control system of a computer system having a CPU provided with a system management mode for accessing a predetermined memory space and a protect mode with a memory addressing method different from the system management mode (col 14 lines 40-44). Arai also teaches a first resume means for executing first resume processing for restoring the status data of the computer system and system management means for managing an operation of the computer system.

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to integrate the teachings of Arai to the teachings of

Kato/Copeland/Tanaka in order to avoid the writing process while data transmission to avoid error in transmission and continue when the transmission of data is over so that the system is not remain paused, but to start up the process again, which utilizes the time efficiently without wasting time.

10. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato as modified by Copeland and Tanaka as applied to claim 1 above, and further in view of Olshansky et al (US 6,061,357). Kato/Copeland/Tanaka have been discussed above.

Kato/Copeland/Tanaka fail to teach wherein the state control circuit includes a time counting circuit for starting counting time in response to the CPU going into halt state, stopping counting the time in response to restoration of the CPU to an operative state and outputting a counted value to the CPU. Kato/Copeland/Tanaka also fail to teach a time monitoring circuit for starting counting time in response to the CPU going into a halt state and outputting a timeout signal to the CPU when the CPU does not restore to an operative state before a counted value reaches a given value and wherein the CPU goes into the operative state in response to the timeout signal output by the time monitoring circuit.

Olshansky teaches a timer that is started by reception of the pause signal and upon expiration of the timeout period, transmission of data packets to ADSL modem is resumed (col 5 lines 47-53).

Therefore, it would have been obvious to an artisan of ordinary sill in the art at the time the invention was made to modify the teachings of Olshansky to the teachings of Kato/Copeland/Tanaka because the buffer memory is limited in memory space and some

memory space must be cleared out before the transmitted data fills up the entire buffer memory, which causes data loss. Therefore, such modification prevents data loss and erroneous data.

Allowable Subject Matter

11. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: The best prior art of record, Kato, Copeland and Tanaka taken alone or in combination fails to teach a normal waveform storing means for storing a waveform pattern standardized by ISO/IEC 14443-3.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kelly, U.S. Patent No 5,787,101, discloses smart card message transfer without microprocessor intervention.

Brickman et al.,U.S. Patent No. 4,315,330, discloses a multiple data rate testing of communication equipment.

Gilbon, U.S. Patent No. 4,814,595, discloses an electronic data communication system.

Goto, U.S. Patent No. 5,670,772, discloses a non-contact data recording medium.

Niimura et al., U.S. Patent No. 5,101,410, discloses a data transmission system for a portable data storage medium.

Iijima, U.S. Patent No. 5,959,276, discloses an issuing customized IC cards of different types.

Tanaka et al., U.S. Patent No. 6,266,810, discloses a remote program downloading system and apparatus.

Bashan et al., U.S. Patent No. 6,161,762, discloses a contact/contactless smart card having customizable antenna interface.

Goto, U.S. Patent No. 6,079,622, discloses a non-contact information storage medium and data transmission method for the medium.

Yorimoto et al., U.S. Patent No. 5,410,714, discloses an integrated-circuit card equipped with a single chip data processor automatically entering low-power consumption mode.

Walton et al., U.S. Patent No. 4,918,416, discloses an electronic proximity identification system.

Mandelbaum, U.S. Patent No. 5,477,215, discloses an arrangement for simultaneously interrogating a plurality of portable radio frequency communication devices.

Snodgrass et al., U.S. Patent No. 5,500,650, discloses a data communication method using identification protocol.

Takahira et al., U.S. Patent No. 5,382,778, discloses a non-contact IC card.

Ohzeki, U.S. Patent No. 4,625,241, discloses timing control signal generator for teletext signal waveform equalizer.

Goto et al., JP 56-96303, discloses a signal waveform storage device.

Matsui et al., JP 4-115614, discloses an automatic equalizer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kumiko C. Koyama whose telephone number is 703-305-5425. The examiner can normally be reached on Monday-Friday 7am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on 703-305-3503. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

kck
January 24, 2003

KARL D. FRECH
PRIMARY EXAMINER